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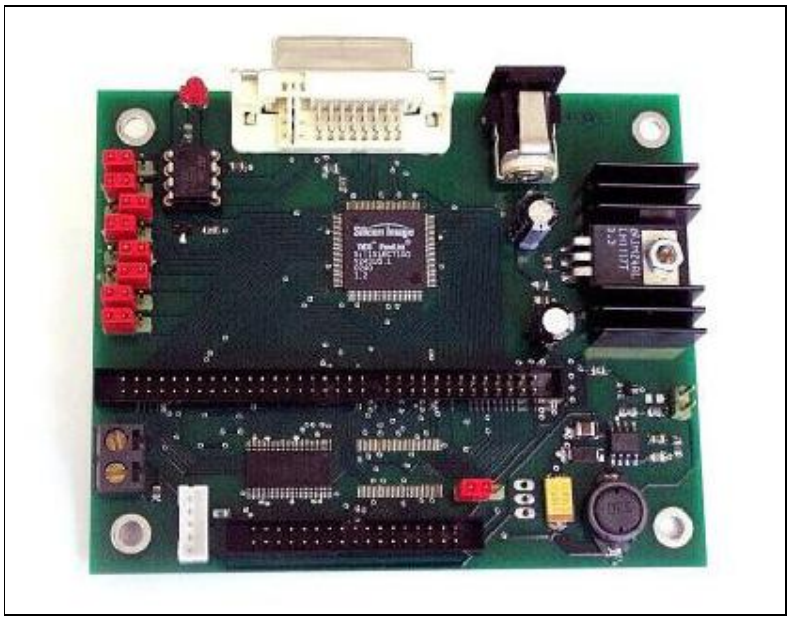
Pr/DVIRec-engl.doc

DVI - Receiver



- **Receiver for driving an LCD panel with TTL or LVDS input with a DVI signal.**
- **On board regulation of the panel supply voltage (3,3V or 5V).**
- **Automatic switch off for panel and backlight when no signal.**

specifications:

power supply	12V +/- 10% 180mA without LVDS backlight und panel
dimensions	100mm x 80mm x 15mm
input	DVI-D receptable
output	TTL 1 or 2 pixel per clock 68pin 2mm grid LVDS 1 or 2 channel 34pin optional Backlight with powerdown and brightness 5pin
plug and play	Hotplug capable EDID 1.3 adapted to the panel
resolution of panel	VGA - UXGA, 25MHz - 165MHz clock, 3x8bit RGB

DVI-receiver
data sheet

technical data:

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dimensions	100mm x 80mm x 15mm
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Power connector

Low voltage connector according to DIN 45323
Pin ∅ 1,9mm
Outside ∅ 6,2mm
Polarity: + inside
Screwed contact with “+”marking on PCB

Backlight connector:

1	+12V
2	GND
3	SyncDetect
4	GND
5	+12V

TTL output:

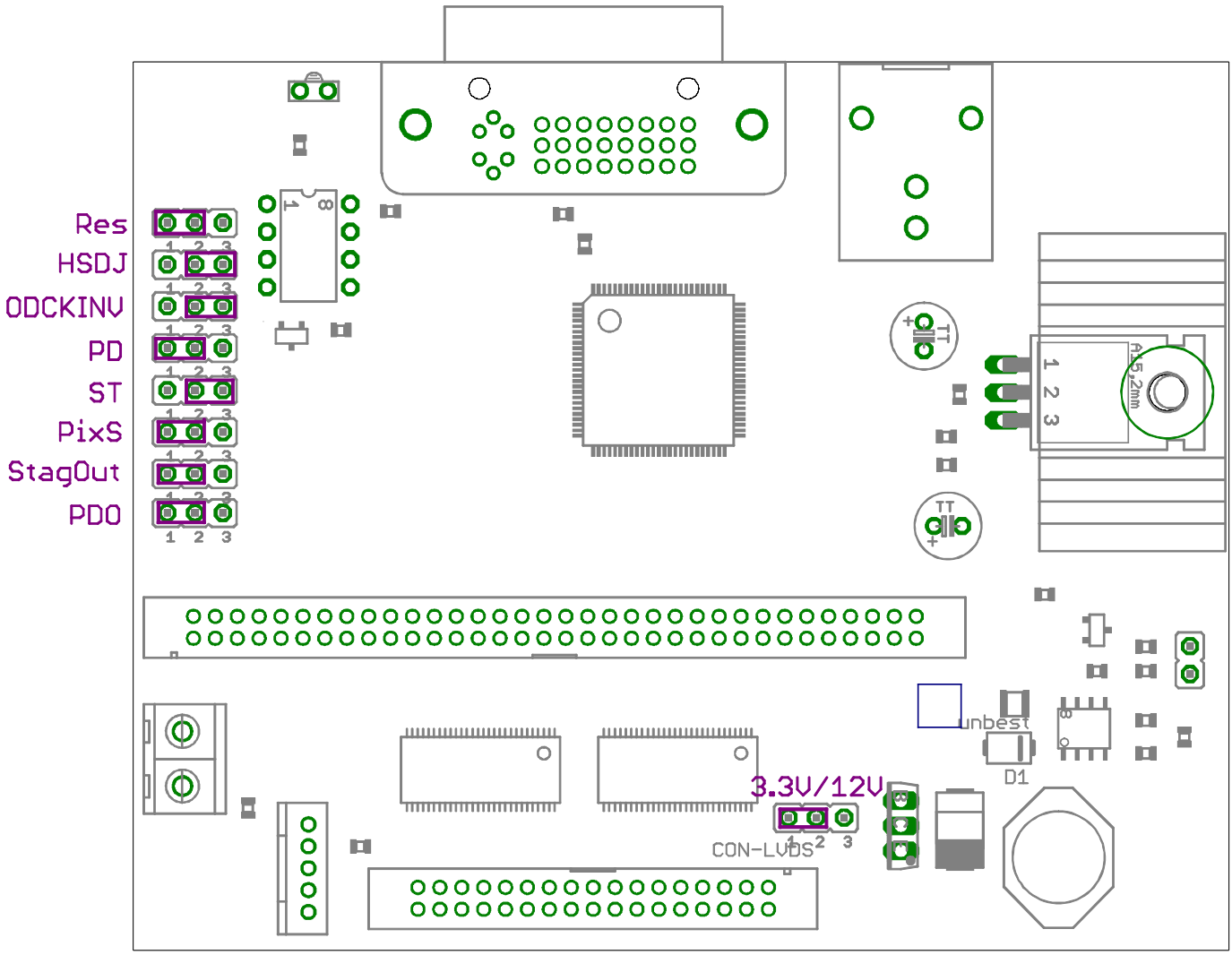
68 pin pinheader with 2mm grid.
for panels with 1 pixel per clock TTL only pins 1 - 40 are required

01	GND	18	EG5	35	GND	52	GND
02	GND	19	EG6	36	HSYNC	53	OG0
03	EB0	20	EG7	37	PanelSupply	54	OG1
04	EB1	21	GND	38	DotClock	55	OG2
05	EB2	22	GND	39	PanelSupply	56	OG3
06	EB3	23	ER0	40	SyncDetect	57	OG4
07	EB4	24	ER1	41	N.C.	58	OG5
08	EB5	25	ER2	42	N.C.	59	OG6
09	EB6	26	ER3	43	OB0	60	OG7
10	EB7	27	ER4	44	OB1	61	OR0
11	GND	28	ER5	45	OB2	62	OR1
12	GND	29	ER6	46	OB3	63	OR2
13	EG0	30	ER7	47	OB4	64	OR3
14	EG1	31	GND	48	OB5	65	OR4
15	EG2	32	DE	49	OB6	66	OR5
16	EG3	33	GND	50	OB7	67	OR6
17	EG4	34	VSYNC	51	GND	68	OR7

LVDS output:

34 pin pinheader im 2mm Raster

01	PanelSupply	18	GND
02	PanelSupply	19	TxA0-
03	PanelSupply	20	TxA0+
04	PanelSupply	21	TxA1-
05	GND	22	TxA1+
06	GND	23	TxA2-
07	TxB0-	24	TxA2+
08	TxB0+	25	TxAclock-
09	TxB1-	26	TxAclock+
10	TxB1+	27	TxA3-
11	TxB2-	28	TxA3+
12	TxB2+	29	GND
13	TxBclock-	30	GND
14	TxBclock+	31	GND
15	TxB3-	32	GND
16	TxB3+	33	GND
17	GND	34	GND


Res
HSDJ
ODCKINV
PD
ST
PixS
StagOut
PDO
3.3V/12V
CON-LVDS
D1
unbest

Jumper description from left to right.

A Jumper set on the outer side of the board provides HIGH level

- **RESERVED**
  Must be tied HIGH for normal operation.

- **HS_DJTR**
  This pin enables/disable the HSYNC dejitter function. To enable the HSYNC function this pin should be tied high. To disable the HSYNC dejitter function and when using in a SiI143 pin to pin application, this pin should be tied low.

- **OCK_INV**
  ODCK(Clock) Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output. All other output signals are not affected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin

- **PD Power Down (active LOW)**
  A HIGH level indicates normal operation. A LOW level indicates power down mode. During power down mode, all the output drivers are put into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. Additionally, all analog logic is powered down, and all inputs are disabled.

- **ST Output Drive**
  A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength. (Doesn´t affect LVDS outputs)

- **PIXS**
  Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.

- **PDO**
  Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO is a sub-set of the PD description. The chip is not in power-down mode with this pin. SCDT and CTL1 are not tri-stated by this pin.

- **STAG_OUT**
  Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in 2-pixels per clock mode.